REMARKS

Claims 1-19 remain pending in this application. Claims 9-19 have been withdrawn from consideration as being directed towards a non-elected invention. Each of the examined claims is believed to define an invention which is novel and unobvious over the cited references. Favorable reconsideration of this case is respectfully requested.

The Title of the Invention has been amended to be clearly indicative of the invention to which the claims are directed.

Submitted herewith on separate sheets are copies of Figure 17-20 labeled "Prior Art" as required by the Examiner.

Claims 1, 3 and 4 have been amended to correct the informalities noted by the Examiner.

The present invention relates to a semiconductor device in which a metal material is embedded in both a wiring groove and a hole used for the contact between lines. In a preferred embodiment, the semiconductor layer comprises an underlayer. A base oxide with holes is formed on the under layer. A plurality of nitride film patterns with a hole pattern are formed on the base oxide film directly above the holes. An upper oxide film is provided on top of the base oxide film to cover the nitride film patterns. The upper oxide film has formed therethrough a plurality of wiring grooves which each exposes part of an associated nitride film pattern including the hole pattern. A wiring metal fills part of the exposed nitride film patterns, the holes and the wiring grooves. The nitride film patterns are formed with such a shape and size to surround the outside of their associated

wiring groove and are separate from neighbouring nitride film patterns. Accordingly, embodiments of the present invention have a nitride film pattern that is only slightly larger than the size of the bottom of the wiring groove and therefore smaller than the total area of the base oxide film. Therefore, the stress placed on the nitride film can be reduced.

Claims 1-8 have been rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Number 5,612,254 to Mu et al. Mu et al. do not anticipate the present invention as it does not disclose, among other things, a plurality of nitride films formed on the base oxide film where the nitride films are separate from neighbouring nitride films as recited in amended claims 1 and 3 or the wiring metal embedded in the wiring groove of the upper oxide film with a first portion having a first diameter and a second portion having a diameter narrower than the first diameter as recited in amended claim 4.

Mu et al. discloses that a silicon nitride film 23 is provided on a BPSG layer 22. An oxide film 50 is provided on the silicon nitride layer 23, column 6, lines 34-49. A titanium nitride barrier layer 60 and a metal layer 61 are embedded in a groove provided in the oxide film 50, column 6, lines 50-63. As shown in Figures 1-11 and described at column 5, line 67 – column 6, line 7, the silicon nitride film 23 is provided on the entire face of the BPGS layer 22 for the wiring groove. There is no disclosure in Mu et al. of providing a plurality of nitride films separately for the plurality of wiring grooves.

In comparison, amended claims 1 and 3 both recite that a plurality of nitride film patterns are formed on the base oxide film. A plurality of wiring grooves are formed to

expose part of an associate nitride film pattern. The nitride film patterns are formed such that they are separate from neighbouring nitride film patterns. For example, in Figure 3 and described at page 8, line 27 – page 9, line 16 of the present specification, a mask used for form the nitride film patterns is described. The mask includes a plurality of line patterns 22 to form the nitride pattern 16 on the base oxide 12, where the nitride patterns are separate from neighbouring nitride patterns, see also page 4, line 8 – page 5, line 7. Accordingly, it is clear the Mu et al. does not disclose each and every element of amended claims 1 and 3.

Claim 4 has been amended to recite that the wiring metal has a first portion around the periphery of the hole having a first diameter and second portion at a middle section of said upper oxide film having a diameter smaller than the first diameter. For example, as shown in Figure 15A and 15B of the present specification, a first portion of the wiring metal is formed on the base oxide film around the periphery of the hole 30. This first portion of the wiring metal has a first diameter that extends outward around the hole 30. A second portion of the wiring metal is arranged above the first portion at a middle section of the upper oxide film 26. At the middle section of upper oxide film, the diameter of the wiring metal is smaller than the first diameter as can be seen by sloping sides of wiring groove 28. Exhibit A is attached hereto to illustrate the first and second portions.

Mu et al. discloses that the titanium nitride barrier layer 60 and the metal layer 61 embedded in the plurality of wiring grooves have approximately the same diameter as the

oxide film 50. There is no disclosure of metal layer 61 having different diameters as recited in amended claim 4. Consequently, it is clear that Mu et al. does not disclose each and every element recited in amended claim 4.

In view of the above discussion, the withdrawal of the rejection of claims 1-8 over Mu et al. is respectfully requested.

Claims 1-8 have been rejected under 35 U.S.C. 102(e) as being anticipated by European Patent Application No. 0892428A2 to Nguyen et al.

Nguyen et al. discloses that a first trench 172 is formed in a first dielectric interlevel 166. A step portion is provided in dielectric 166 with a second barrier layer 178 formed in the surface of the step portion, a second metal level 188 is embedded in the first trench as illustrated in Figures 14-18. The first trench 172 is formed entirely in one dielectric interlevel 166, column 10, lines 36-57. Nguyen et al. does not include a base oxide film or an upper oxide film as is recited in claims 1, 3 and 4 of the present invention.

Additionally, each of claims 1 and 3 recite that the upper oxide film is provided on top of the base oxide film to cover the nitride film pattern. Nguyen et al. merely describes that the second barrier layer 178 is provided on the step portion. There is no disclosure that the nitride film is covered by the upper oxide film. In fact, what the Examiner contends is upper oxide film 170 does not cover second barrier layer 178 as shown in Figures 14-18 of Nguyen.

Furthermore, amended claim 4 recites that the wiring metal has first and second portions with the second portion having a diameter at a middle section of the upper oxide film that is smaller than the diameter of the wiring metal in the first portion. There is no disclosure in Nguyen et al. of this feature.

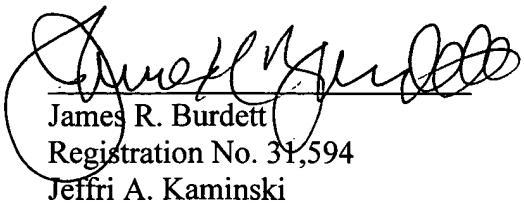
In view of the above discussion, it is clear that the cited reference does not disclose each and every element recited in the amended claims as is required by 35 U.S.C. 102(e). Therefore, the withdrawal of this rejection is respectfully requested.

If the Examiner is of the opinion that the prosecution of this application would be advanced by a personal interview, the Examiner is invited to telephone undersigned counsel to arrange for such an interview.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Commissioner is authorized to charge any fee necessitated by this Amendment to our Deposit Account No. 22-0261.

Respectfully submitted,



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VERSION SHOWING CHANGES MADE

IN THE SPECIFICATION:

Please amend the Title of the Invention as follows:

SEMICONDUCTOR DEVICE ~~AND SEMICONDUCTOR MANUFACTURING METHOD~~WITH REDUCED INTERCONNECTION CAPACITY

Please replace the third full paragraph on page 5 with the following rewritten paragraph:

Figure 1(A) to 1(C) are diagrams that overview the processes involved in the manufacture of a semiconductor in a first embodiment of the present invention and shows a cross-section through the structure;

IN THE CLAIMS:

Please amend the claims as follows:

1. A semiconductor device, comprising:

~~a~~ an underlayer;

a base oxide film with holes and formed on the underlayer;

a plurality of nitride film ~~pattern~~ patterns with a hole pattern formed on the base oxide film and directly above said holes;

an upper oxide film provided on top of said base oxide film to cover the nitride film ~~pattern~~ patterns, the upper oxide film having formed therethrough ~~a~~ an

plurality of wiring ~~groove~~ grooves which each exposes part of ~~the~~ an associated nitride film pattern including said hole patterns; and

wiring metal that fills part of the exposed nitride film ~~pattern~~ patterns, said holes, and said wiring grooves;

and wherein said nitride film ~~pattern~~ patterns ~~is~~ are formed with such a shape and size that surrounds the outside of ~~said~~ their associated wiring groove and ~~is~~ are separate from neighbouring nitride film patterns.

3. A semiconductor device, comprising:

~~a~~ an underlayer;

a base oxide film with holes formed on the underlayer;

a plurality of nitride film ~~pattern~~ patterns with a hole pattern provided on the base oxide film and formed directly above said holes;

an upper oxide film provided on top of said base oxide film to cover the nitride film patterns, the upper oxide film having formed therethrough a plurality of wiring ~~groove~~ grooves which each exposes part of ~~the~~ an associated nitride film pattern including said hole patterns; and

wiring metal that fills part of the exposed nitride film pattern, said holes, and said wiring grooves;

and wherein outer shape of said nitride film pattern is substantially the same as the shape of the opening of said wiring groove, ~~and wherein~~ an internal wall

surface of said wiring groove is tapered from the opening on the upper surface of said upper oxide film to upper surface of said nitride film pattern and neighbouring nitride film patterns are separate from each other.

4. A semiconductor device, comprising:

~~a~~ an underlayer;

a base oxide film formed on the underlayer, the base oxide film having formed therethrough a plurality of holes;

an upper oxide film provided on the base oxide film, the upper oxide film having formed therethrough wiring grooves which are connected to said holes; and

wiring metal that fills said holes and said wiring grooves, said wiring metal having a first portion around the periphery of said hole having a first diameter and a second portion at a middle section of said upper oxide film above said first portion having a diameter smaller than the first diameter.

USSN 09/736,140

reference drawing Exhibit A

FIG. 15(A)

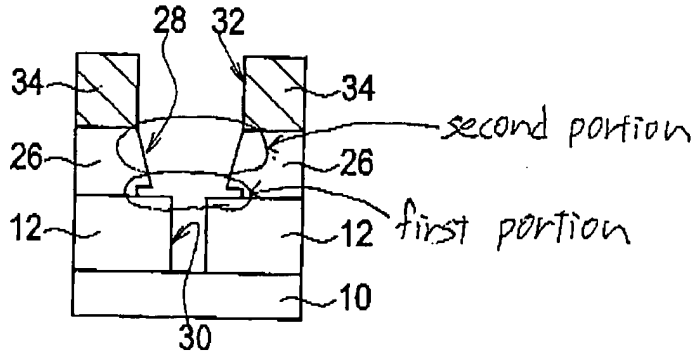

FIG. 15(B)